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10/684,793	10/13/2003	Yervant Zorian	4640P020	4222

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
NGUYEN, STEVE N	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/684,793	ZORIAN ET AL.	
	Examiner	Art Unit	
	Steve Nguyen	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 are pending and have been considered.

Drawings

2. The amended drawings are accepted. The objection to the drawings in the first office action is withdrawn.

Claim Objections

3. In view of the amended claims, all objections in the prior Office Action are withdrawn.

Claim Rejections - 35 USC § 112

4. The U.S.C. 112, second paragraph rejection of claims 5, 7, 13, 15, 20, and 26 has been withdrawn in view of the amended claims.

Response to Arguments

5. Applicant's arguments filed 1/8/2007 with respect to claims 1-26 and 33, 34, 37, and 38 have been fully considered but they are not persuasive. Applicant's arguments with respect to claims 27-32 and 35-36 have been considered but are moot in view of the new ground(s) of rejection.

The Applicants argue that Weiss does not disclose a single on chip processor coupled and configured to repair multiple discrete memory cores, and thus the combination of Anand and Weiss would lack an on-chip processor testing multiple memory cores.

The Examiner asserts that Weiss in view of Anand teaches all of the claim limitations. Claim 1 recites in part:

- "two or more memories having one or more redundant components associated with each memory" and
- "a first processor containing redundancy allocation logic to execute one or more repair algorithms to generate a repair signature for each memory".

Turning to Fig. 6 of Weiss, two or more memories are shown as reference numbers 700, 701, and 702. These memories are referred to as "memory segments" by Weiss. Each of these memory sub-blocks contributes to the total amount of memory in the memory structure 600 (see col. 9, lines 13-22). A first processor to execute one or more repair algorithms to generate a repair signature for each memory is clearly taught by Weiss in col. 16, lines 12-20. The single processor recited by Weiss generates a repair signature for each of the memory sub-blocks 700, 701, and 702 in the repairable memory structure 600. Therefore the claim limitation is met.

The Applicants argue that Anand does not disclose a single on chip processor coupled and configured to repair multiple discrete memory cores, but rather Anand teaches away from this concept.

The Examiner would like to point out that Anand does not discuss testing and programming with an external testing unit and not an on-chip processor, as alleged by Applicants. Furthermore, Applicants have misread Anand, stating that Anand teaches "the IC field of art's concern about the limited area available on a chip to place components". The disclosure of Anand has nothing to do with the limited area available on a chip to place components, but rather is directed to the placement and use of fuses in a memory for repairing the memory that overcome the difficulties in programming fuses of the prior art.

Applicants cited col. 3, lines 43-51 for support of this argument. However, the cited passage only states that the invention of Anand overcomes the deficiencies of programming prior art fuses. One of these deficiencies is that laser-programmable fuses require a large guard ring in order to protect surrounding circuitry. This still has nothing to do with the limited area available on a chip to place components. Anand is not mainly concerned with the problem of limited area available on a chip, as this problem only occurs with laser-programmable fuses (col. 1, lines 66-67). Anand is concerned with the numerous problems associated with all of the prior art fuse types, such as damaging components by local heating (col. 1, lines 65-66), damaging wires in a deep stack configuration (col. 2, lines 4-8), and fuses which are not registered as being blown (col. 2, lines 27-31). Finally, one of ordinary skill in the art at the time the invention was made to would have recognized that a control processor would have been necessary in the IC 10 of Anand for controlling operations. For example, at least

the scan registers would have required control by a processor for switching into a serial test configuration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-21, 27, 28, 30, 31, 35, and 37 rejected under 35 U.S.C. 103(a) as being unpatentable over Weiss et al (US Pat. 6,249,465; hereinafter referred to as Weiss) in view of Anand et al (US Pat. 6,577,156; hereinafter referred to as Anand).

See the Non-Final Action filed 10/4/2004 for a detailed action of prior rejections.

7. Claims 22-26 and 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Anand.

See the Non-Final Action filed 10/4/2004 for a detailed action of prior rejections.

8. Claims 34 and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of Rona (US Pat. 5,350,940).

See the Non-Final Action filed 10/4/2004 for a detailed action of prior rejections.

9. Claims 27-32 and 35-36 rejected under 35 U.S.C. 103(a) as being unpatentable over Weiss in view of Anand in view of Reed (US Pat. 5,204,836).

As per claims 27 and 28:

Weiss teaches a method, comprising:

- composing a repair signature for two or more memory cores (col. 11, lines 26-33);
- sending the repair signature for each memory core to be stored in non-volatile fuses (col. 11, lines 26-33);
- storing an actual repair signature for a subset of the two or memories (col. 11, lines 26-33) and a dummy repair signature for the remaining memories (col. 11, lines 43-46).

Not explicitly disclosed by Weiss is decompressing the repair signature for each memory core to send reconfiguration data to the two or more memories. However, Anand in an analogous art teaches decompressing data in a fuse box (col. 3, lines 54-58). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the decompressor of Anand with the circuit of Weiss. This modification would have been obvious to one of ordinary skill in the art, at

the time the invention was made, because one of ordinary skill in the art would have recognized that a compressor and decompressor would have saved space.

Not explicitly disclosed by Anand or Weiss is composing a repair signature for two or more memory cores on every cycle a device containing the two or more memory cores is initialized. However, Reed in an analogous art teaches checking and repairing memories upon each power-up sequence (col. 8, line 56-col. 9, line 4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to conduct a test of the memory on every cycle a device is initialized. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that conducting a test of the memory on each cycle a device is initialized is a common way to resolve a fault before the device is to be operated (col. 8, lines 56-65).

As per claim 29:

Anand teaches the method of claim of 27, further comprising: repairing an adjustable subset of memory cores having redundant elements (abstract).

As per claims 30 and 31:

Weiss teaches an apparatus, comprising:

- means for composing a repair signature for two or more memories (col. 11, lines 26-33);
- means for sending the repair signature to be stored in non-volatile fuses (col. 11, lines 26-33); and

- means for storing an actual repair signature for a subset of the two or memories (col. 11, lines 26-33) and a dummy repair signature for the remaining memories (col. 11, lines 43-46).

Not explicitly disclosed by Weiss is means for decompressing the repair signature to send reconfiguration data to the two or more memories. However, Anand in an analogous art teaches decompressing data in a fuse box (col. 3, lines 54-58). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the decompressor of Anand with the circuit of Weiss. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that a compressor and decompressor would have saved space.

Not explicitly disclosed by Anand or Weiss is composing a repair signature for two or more memory cores on every cycle a device containing the two or more memory cores is initialized. However, Reed in an analogous art teaches checking and repairing memories upon each power-up sequence (col. 8, line 56-col. 9, line 4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to conduct a test of the memory on every cycle a device is initialized. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that conducting a test of the memory on each cycle a device is initialized is a common way to resolve a fault before the device is to be operated (col. 8, lines 56-65).

As per claim 32:

Anand teaches the apparatus of claim of 30, further comprising: means for repairing an adjustable subset of memories having redundant elements (abstract).

As per claim 35:

Weiss teaches:

- two or more memories having redundant components that share the repair data container (Fig. 6, elements 700-715), wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the two or more memories (col. 9, lines 36-38).

Not explicitly disclosed by Weiss is a repair data container located on a chip, the repair data container to store an actual repair signature for each memory having a defect. However, Anand in an analogous art teaches a repair data container (Fig. 1, element 11), and Weiss teaches elements designed to store an actual repair signature for the memories (col. 11, lines 26-33).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the elements of Weiss shown in Fig. 6 into a repair data container such as the one disclosed by Anand. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because it has been held that integrating together a plurality of pieces involves only routine skill in the art. *In re Larson* 144 USPQ 347 (CCPA 1965).

Not explicitly disclosed by Anand or Weiss is composing a processor having logic configured to test the memory cores during each cycle of operation and to generate an augmented repair signature if a new defect is detected. However, Reed in an

analogous art teaches checking and repairing memories upon each power-up sequence (col. 8, line 56-col. 9, line 4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to conduct a test of the memory on every cycle a device is initialized. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that conducting a test of the memory on each cycle a device is initialized is a common way to resolve a fault before the device is to be operated (col. 8, lines 56-65).

10. Claim 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of Weiss in view of Reed in view of Rona (US Pat. 5,350,940).

As per claim 36:

Weiss, Anand, and Reed teach the machine-readable medium of claim 35 above. Not explicitly disclosed is wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the repair data container and the two or more memories. However, Rona teaches fabrication of semiconductors using lithographic masks (col. 8, lines 35-38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a lithographic mask. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made,

because one of ordinary skill in the art would have recognized that fabrication using lithographic masks is well known (col. 8, lines 35-38).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steve Nguyen
Examiner
Art Unit 2138